AbstractPlus | References | Full Text: PDF(424 KB) IEEE JNL
Rights and Permissions

6. **Loop Scheduling for Multithreaded Processors**
Dimitriou, G.; Polychronopoulos, C.;
Parallel Computing in Electrical Engineering, 2004. PARELEC 2004. International Conference on
7-10 Sept. 2004 Page(s):361 - 366
Digital Object Identifier 10.1109/PCEE.2004.42
AbstractPlus | Full Text: PDF(208 KB) IEEE CNF
Rights and Permissions

7. **A study of the on-chip interconnection network for the IBM Cyclops64 multi-core architectu**
Ying Ping Zhang; Taikyeong Jeong; Fei Chen; Haiping Wu; Nitzsche, R.; Gao, G.R.;
Parallel and Distributed Processing Symposium, 2006. IPDPS 2006. 20th International
25-29 April 2006 Page(s):10 pp.
Digital Object Identifier 10.1109/IPDPS.2006.1639301
AbstractPlus | Full Text: PDF(184 KB) IEEE CNF
Rights and Permissions

8. **Designing and evaluating network processor applications**
Jing Fu; Hagsand, O.;
High Performance Switching and Routing, 2005. HPSR. 2005 Workshop on
12-14 May 2005 Page(s):142 - 146
Digital Object Identifier 10.1109/HPSR.2005.1503211
AbstractPlus | Full Text: PDF(334 KB) IEEE CNF
Rights and Permissions

9. **Loop scheduling for multithreaded processors**
Dimitriou, G.; Polychronopoulos, C.;
Parallel Computing in Electrical Engineering, 2004. International Conference on
7-10 Sept. 2004 Page(s):361 - 366
Digital Object Identifier 10.1109/PCEE.2004.1335651
AbstractPlus | Full Text: PDF(343 KB) IEEE CNF
Rights and Permissions

10. **Inexpensive throughput enhancement in small-scale embedded microprocessors with block extensions, characterization, and tradeoffs**
Haskins, J.W., Jr.; Hirst, K.R.; Skadron, K.;
Performance, Computing, and Communications, 2001. IEEE International Conference on.
4-6 April 2001 Page(s):319 - 328
Digital Object Identifier 10.1109/IPCCC.2001.918669
AbstractPlus | Full Text: PDF(976 KB) IEEE CNF
Rights and Permissions

11. **Micro-threading: a new approach to future RISC**
Jesshope, C.; Luo, B.;
Computer Architecture Conference, 2000. ACAC 2000. 5th Australasian
31 Jan.-3 Feb. 2000 Page(s):34 - 41
Digital Object Identifier 10.1109/ACAC.2000.824320
AbstractPlus | Full Text: PDF(136 KB) IEEE CNF
Rights and Permissions

12. **Datarol: a parallel machine architecture for fine-grain multithreading**
Amamiya, M.; Tomiyasu, H.; Kusakabe, S.;
Massively Parallel Programming Models, 1997. Proceedings. Third Working Conference on
12-14 Nov. 1997 Page(s):151 - 162
Digital Object Identifier 10.1109/MPPM.1997.715971
AbstractPlus | Full Text: PDF(1132 KB) IEEE CNF

Rights and Permissions

13. **The compiler for supporting multithreading in cyclic register windows**
Li Cheng; Wang Dingxing; Shen Meiming; Zheng Weimin; Peng Shanling;
Parallel Architectures, Algorithms, and Networks, 1996. Proceedings, Second International Sympo:
12-14 June 1996 Page(s):57 - 62
Digital Object Identifier 10.1109/ISPAN.1996.508961
AbstractPlus | Full Text: PDF(524 KB) IEEE CNF
Rights and Permissions

14. **The EM-X parallel computer: architecture and basic performance**
Kodama, Y.; Sakane, H.; Sato, M.; Yamana, H.; Sakai, S.; Yamaguchi, Y.;
Computer Architecture, 1995. Proceedings, 22nd Annual International Symposium on
22-24 Jun 1995 Page(s):14 - 23
AbstractPlus | Full Text: PDF(868 KB) IEEE CNF
Rights and Permissions

15. **Fine-grain multi-thread processor architecture for massively parallel processing**
Kawano, T.; Kusakabe, S.; Taniguchi, R.-I.; Amamiya, M.;
High-Performance Computer Architecture, 1995. Proceedings, First IEEE Symposium on
22-25 Jan. 1995 Page(s):308 - 317
Digital Object Identifier 10.1109/HPCA.1995.386532
AbstractPlus | Full Text: PDF(452 KB) IEEE CNF
Rights and Permissions

Indexed by Inspec®